CAPACITIVE ADIABATIC LOGIC:
A NEW PARADIGM FOR LOW-POWER COMMUTATION

Microenergy, Gubbio, Italy
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ENERGY DISSIPATION IN DIGITAL ELECTRONICS CIRCUITS

Power density issue
CMOS-based digital circuit in nano-scaled technology consume <1kW/cm²*
10x higher than air cooling dissipation capability
⇒ recent technologies offer billions of transistors but cannot be used at the same time!

Energy issue
Comparing to Landauer limits (3zJ@300k),
one logic operation in deep CMOS technology node costs x10⁵ more

Why do we need to dissipate high amount of energy to code one logic state in current digital circuit using CMOS technology?

* considering buffer gate on \(10^{-2} \text{ µm}^2\) with 0.1fF gate capacitance operating at 1GHz
** considering 1 zetta flops and 50W
CMOS BASED LOGIC ROOT LIMITATION #1

Go back to the energy transfer basic in a elementary inverter logic gate

Energy provided by energy source to code one logic bit:

\[ E_{V_{DC}} = \int_{t=0}^{T_{OP}} U_{DC} \times I_{DC} = C_G V_{CC}^2 \]

\( NB: R_{ON} \) value has not effect

Classical digital circuits suffer from inherent dynamic loss (not device dependent) due to sharp transition between two logic states
CMOS BASED LOGIC ROOT LIMITATION #1

Is it really a serious problem?

Quantify this inherent loss in the last node CMOS technology:

\[ \{V_{CC};C_G^+\} = \{1V;0.1fF\} \Rightarrow E_{OP} = 0.1fJ >> 3zJ \text{ given by Landauer limit: } k_B.T.\ln(2) \]

Yes! we are x10^5 far from the minimal energy to code one bit!

Does the CMOS scaling help?

Move to the next lower node: \( C_G/2 \) & \( V_{CC} \sim \text{cst} \Rightarrow E_{OP}/2 \text{ per node…} \)

Does the subthreshold operation help?

\( V_{CC} \sim 0.3V \Rightarrow E_{OP}/10… \text{ and higher leakage (see later)} \)

Scaling or subthreshold cannot fill the huge gap

* best case: interconnections cap’ is assumed equal to zero
WHAT’S NEXT?

The huge energy gap to fill needs a hardware revolution!

Fortunately, the *adiabatic* technique has been introduced to avoid a hardware revolution…

**Basic idea:**
only replace a DC-power supply $V_{DC}$ by a trapezoidal power-clock $V_{PC}$
ADIABATIC ENERGY GAIN AND LIMITATION WITH FET

Go back to the energy transfer basic, but with “soft charging”

\[ E_{V_{PC}} = \int_{t=0}^{T_{OP}} U_{PC} \times I_{PC} \approx \frac{R_{ON} C_{G}}{T_{RAMP}} C_{G} (V_{CC}^2 - V_{TH}^2) + \frac{C_{G} V_{TH}^2}{T_{RAMP} \gg R_{ON} C_{G}} \]

Controlled inherent *dynamic loss* in adiabatic

Uncontrolled inherent *dynamic loss* due to the FET behavior
It it really a serious problem?

Quantify this uncontrolled loss in the last node CMOS technology:
\{V_{CC};C_G\}={1V;0.1fF}
\{R_{ON};T_{RAMP}\}={1k\Omega;10ps}
\(V_{TH}=0.3V\)  \(\Rightarrow\)  \(E_{OP}=0.01fJ >> 3zJ\)

Yes! we are \(10^4\) higher than the Landauer limit

Why not reduced \(V_{TH}\)?

Because we are face to a hardware limitation…

\[ E_{VP_C} \approx \frac{R_{ON}C_G}{T_{RAMP}} C_G (V_{CC}^2 - V_{TH}^2) + C_G V_{TH}^2 + I_{OFF}V_{CC}T_{RAMP} \]

\(\underbrace{\text{dynamic loss } f(V_{TH})}_{\text{static loss } f\left(\frac{1}{V_{TH}}\right)}\)

An inherent trade-off for any semiconductor device between its cut-off and on-state strength exits
WHAT’S NEXT?

Adiabatic technique is efficient but not using FET devices. We need a hardware revolution!

Fortunately, the *mechanical device* has been (re)introduced*…

Basic idea:
Use metal contact (or no contact) to have not $I_{ON}$ over $I_{OFF}$ compromise

* * in combination with adiabatic technique
HOW TO FABRICATE RELAYS?

ENERGY DISSIPATION USING MEMS RELAYS

\[ E_{VP} = \int_{t=0}^{TOP} U_{PC} \times I_{PC} \approx \frac{R_{ON} C_G}{T_{RAMP}} C_G (V_{CC}^2 - V_{PO}^2) + \frac{C_G V_{PO}^2}{T_{RAMP} \gg R_{ON} C_G} C_G V_{PO}^2 \]

Controlled inherent *dynamic loss* in adiabatic

Still uncontrolled inherent *dynamic loss* in adiabatic based on relay

Quantify for nano-scale relay:
- \{U_{PI}; U_{PO}\} = \{10mV; 1mV\}
- \{V_{CC}; C_G\} = \{1V; 100pF\}
- \{R_{ON}; T_{RAMP}\} = \{10k\Omega, 100\mu s\} \implies E_{OP} = 0.1fJ

No, we are still \(10^4\) higher than the Landauer limit with \(x10^{10}\) operating period and \(x10^6\) size compared to MOS

+ technological limitation:
  mechanical reliability due to the bad electrical contact and chocks…
WHAT’S NEXT?

Go back to our old MOS transistors or try another revolution to save energy?

Fortunately, the capacitive adiabatic logic is introduced! [1]

Basic idea: use relay but in (electrical) contactless operation and adiabatic operation

HOW TO USE CONTACTLESS RELAYS?

Relays become variable capacitors in CAL paradigm

Buffer example

"0" logic input

\[ V_o = \frac{R_{ON}}{R_{OFF} + R_{ON}} V_{PC} \sim 0 \]

"1" logic input

\[ V_o = \frac{R_{OFF}}{R_{OFF} + R_{ON}} V_{PC} \sim V_{PC} \]

Trade resistive divider for capacitive one

\[ V_o = \frac{C_L}{C_H + C_L} V_{PC} \sim 0 \]

\[ V_o = \frac{C_L}{C_L + C_H} V_{PC} \sim V_{PC} \]
WHO IS THE ELEMENTARY DEVICES IN CAL?

Positive- and negative- variable capacitors (VC) are the elementary hardware device in CAL.

<table>
<thead>
<tr>
<th>MOS</th>
<th>relay</th>
<th>VC</th>
</tr>
</thead>
<tbody>
<tr>
<td>P-MOS</td>
<td></td>
<td>P-CV</td>
</tr>
<tr>
<td>N-MOS</td>
<td></td>
<td>N-CV</td>
</tr>
</tbody>
</table>

Analogy to transistor-, relay-based logic

\[ P-CV C(V) \text{ curve} \]

\[ N-CV C(V) \text{ curve} \]
How to change a capacitor value?

\[
C_{DS} = \varepsilon_0 \varepsilon_r \frac{w \times l}{g}
\]

By changing surface \((w \times l)\), gap between plates \((g)\) or permittivity \((\varepsilon_r)\).

\(C_{DS}\) changes by an isolated voltage \(U_{GB}\)

\(\Rightarrow\) it is a four terminals device

Actuation could be:

- Thermal \(\Rightarrow\) not very reversible…
- Piezoelectric \(\Rightarrow\) trade off between leakage and dynamic losses
- Electrodynamic \(\Rightarrow\) current actuation
- Electrostatic \(\Rightarrow\) small gap needed to have reasonable supply voltage
PROPOSED HARDWARE SOLUTION*

Well known MEMS topology (excepted isolation)
Electrostatic actuation using comb drive in both sides
Purely “contact-less” (electrical & mechanical)

* This is not the only hardware solution to implement a 4-terminal variable cap’
DISPLACEMENT AGAINST INPUT VOLTAGE

“low” position

“high” position ($V_{GB}>0$)

Simulation from Coventor, MEMS+
ELECTROMECHANICAL CHARACTERISTICS

The MEMS sizing is given by cascability logic constraints (see later)

Displacement against input voltage

Capacitance vs input voltage

\[ i(t) = C(x) \frac{dV(t)}{dt} + \frac{dC(x)}{dx} V \frac{dx}{dt} \]

Simulation from Coventor, MEMS+ for 1mm² device (2µm gap)
BUFFER BEHAVIOR: STEP BY STEP

Buffer pipeline

\[ V_{PC1} \quad V_{PC2} \quad V_{PC3} \quad V_{PC4} \]

Waiting Evaluation Holding Recovery

Waiting

\[ V_{in3} \]

PC2 provides energy to VC

Evaluation

\[ V_{PC3} \]

PC3 waits the input

\[ C_{out3,Low} \] \( \alpha C_{out3} \] \( C_{out3,High} \]

PC3 provides energy to VC

Holding

\[ C_{out3,High}/(C_{out3,High}+C_{in4}) \times V_{PC3} \]

PC2 recovers energy to VC

Recovery

\[ V_{out3} \]

PC3 recovers energy to VC

\[ i_{PC3} \]

PC3 also recovers energy to VC

\[ PCs \ have \ a \ \pi/2 \ phase \ shift \]
BUFFER BEHAVIOR: ENERGY TRANSFER

$\text{elec. energy from/to } PC_{i-1}$

$\text{energy in the variable capacitor } VC_i$

$\text{elec. energy from/to } PC_i$

$\text{loss from power supply}$

$\text{loss inside material}$

$\text{spring energy } 1/2kx^2$

$\text{elec. cap’ energy } 1/2C_{in}V_{in}^2 + 1/2C_{out}V_{out}^2$

$\text{kinetic energy: } 1/2mdx/dt^2$

$\text{viscosity loss } \alpha dX_i/dt$

$\text{chock loss}$

$\text{contactless}$

$\text{[in green] loss controlled by the ramping time } T \uparrow \Rightarrow E_{loss} \downarrow$

$\text{resistive loss } \alpha I_i^2$

$\text{loss from power supply}^*$

$\text{loss inside material}$

$\text{contactless}$

$\text{* Power supply must be reversible and AC (literature has already proved high efficiency power supplies)}$
(OUR) "ADIABATIC LOSS" DEFINITION

Definition: loss scaling linearly with the ramping time

Need low dissipation? Reduce the speed!

Here, our MEMS moving is always controlled by the power clock ramping time

“Gap closing” MEMS is not suitable as motion is not controlled after the pull-in
ENERGY ANALYSIS OF ELEMENTARY MOVING

\[ E_{OP,\text{min}} = 1.2 \text{pJ} \text{ pour } 1\text{mm}^2 \]

(vs 1fJ for nano-scale transistor)

thanks to the controlled moving and energy back
The biggest issue: find the right MEMS configuration (cap variation, $C_{in}$ vs $C_{out}$…) to propagate the logic state gate by gate

Cascability condition
= have different voltage levels
Occurred when $30V < V_{PC} < 37V$
LOGIC OPERATION: OR EXAMPLE

All combination logic operation is possible with CVP and/or CVN devices.
Based on the current (first draft) MEMS...

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gap</td>
<td>$1/k$</td>
</tr>
<tr>
<td>Linear sizes</td>
<td>$1/k$</td>
</tr>
<tr>
<td>Mass</td>
<td>$1/k^3$</td>
</tr>
<tr>
<td>Spring constant</td>
<td>$k$</td>
</tr>
<tr>
<td>Frequency</td>
<td>$k$</td>
</tr>
<tr>
<td>Capacitance</td>
<td>$1/k$</td>
</tr>
<tr>
<td>Actuation voltage</td>
<td>$1/k$</td>
</tr>
<tr>
<td>$E_{\text{LOSS}}$</td>
<td>$1/k^3$</td>
</tr>
</tbody>
</table>

** ROADMAP FOR DEEPER INTEGRATION **

- **$E_{\text{OP}}$ [J]**
  - $2\mu$m: 1p
  - 200nm: 1f
  - 20nm: 1a
  - 2nm: 1z

- **$S_{\text{si}}$ [$\mu$m$^2$]**
  - $2\mu$m: $10^5$
  - 200nm: $10^4$
  - 20nm: $10^3$
  - 2nm: $10^2$

- **$F_{\text{op}}$ [MHz]**
  - $2\mu$m: 0.1
  - 200nm: 1
  - 20nm: 10
  - 2nm: 100

**Energy gain** $\times 10^5$

**Surface penalty** $\times 10^4$

**Speed penalty** $\times 10$

**Targeted application:** low processing rate with high energy constraint (e.g. autonomous environmental sensors)
THANKS TO THE TEAM

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Gregory Snider  Samer Houri  Ayrat Galisultanov  Yann Perrin

Prof. Univ. of Notre Dame  Delft Tech. Univ.  post doc.  post doc.

External partners

Post PhD
CONCLUSION

Actual CMOS logic is an “energy heresy” for logic operation
The root of the problem is the elementary gate behavior

⇒ New device / design style at the gate level has to be invented!

Adiabatic design style is promising but we need a dedicated device, not FET

⇒ variable capacitor (VR) seems to be “adiabatic compatible”

This is preliminary results waiting the silicon device measurements…

Contact-less variable capacitors could be based on:
- well-known MEMS structures with already proved scalability and reliability abilities
- Other (reversible) actuation: to be defined!

Beware: every solution has to be cascadable (propagate logic state to the next stage)

It is not a crazy alternative to reduce the energy dissipation…

Open question: where is the energy limit using the proposed MEMS?

Your feedbacks are more than welcome!
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