CAPACITIVE ADIABATIC LOGIC: A NEW PARADIGM FOR LOW-POWER COMMUTATION

Microenergy, Gubbio, Italy
Gaël Pillonnet | July 2017

ENERGY DISSIPATION IN DIGITAL ELECTRONICS CIRCUITS

Power density issue

CMOS-based digital circuit in nano-scaled technology consume <1kW/cm^2*

10x higher than air cooling dissipation capability

➔ recent technologies offer billions of transistors but cannot be used at the same time!

Energy issue

Comparing to Landauer limits (3zJ@300k),

one logic operation in deep CMOS technology node costs x10^5 more

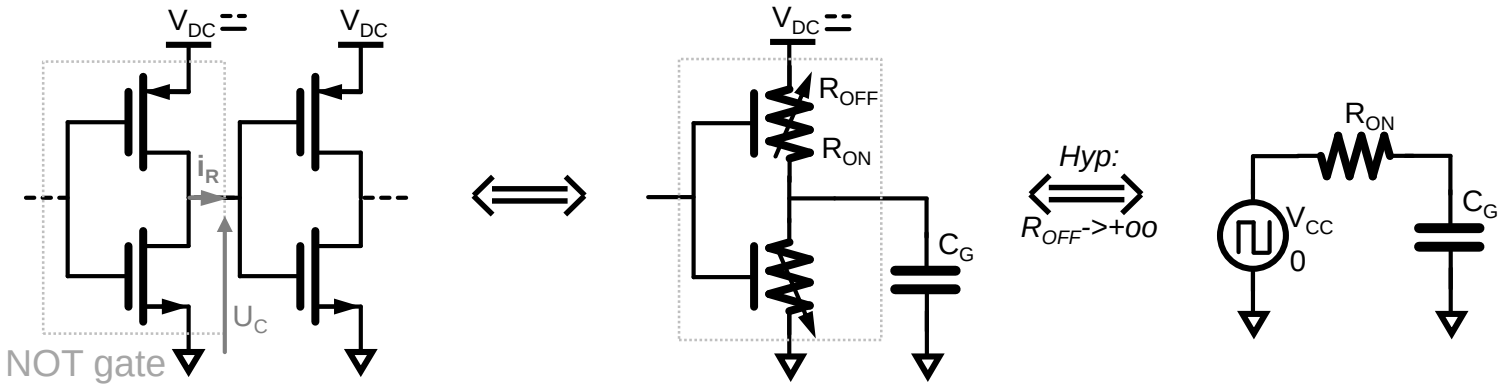
Why do we need to dissipate high amount of energy to code one logic state in current digital circuit using CMOS technology ?

** considering buffer gate on 10^{-2} µm^2 with 0.1fF gate capacitance operating at 1GHz*

*** considering 1 zetta flops and 50W*

CMOS BASED LOGIC ROOT LIMITATION #1

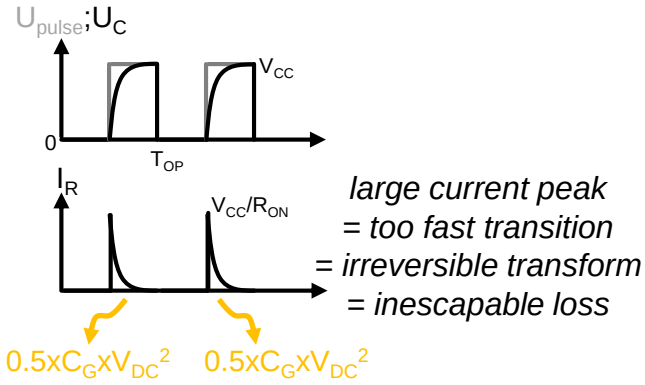
Go back to the energy transfer basic in a elementary inverter logic gate



Energy provided by energy source to code one logic bit:

$$E_{V_{DC}} = \int_{t=0}^{T_{OP}} U_{DC} \mathrm{x} I_{DC} = C_G V_{CC}^2$$

NB: R_{ON} value has not effect



Classical digital circuits suffer from <u>inherent</u> *dynamic loss*
(not device dependent)
due to sharp transition between two logic states

CMOS BASED LOGIC ROOT LIMITATION #1

Is it really a serious problem?

Quantify this inherent loss in the last node CMOS technology:

$\{V_{CC};C_G^*\}=\{1V;0.1fF\}$ ➔ $E_{OP}=0.1fJ >> 3zJ$ given by Landauer limit: $k_B.T.\ln(2)$

Yes! we are x10^5 far from the minimal energy to code one bit!

Does the CMOS scaling help?

Move to the next lower node: $C_G/2$ & V_{CC}~cst ➔ $E_{OP}/2$ per node…

Does the subthreshold operation help?

V_{CC}~0.3V ➔ $E_{OP}/10$… *and higher leakage (see later)*

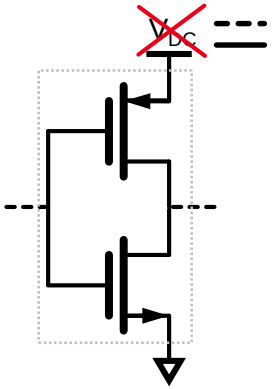
Scaling or subthreshold cannot fill the huge gap

** best case: interconnections cap' is assumed equal to zero*

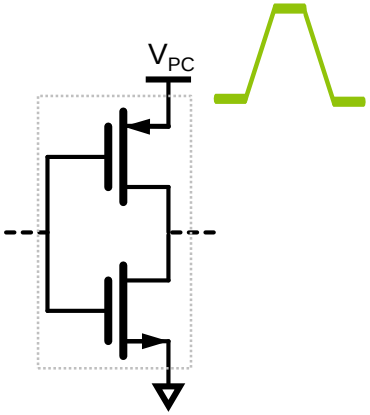
WHAT'S NEXT?

The huge energy gap to fill needs a hardware revolution!

Fortunately, the *adiabatic* technique has been introduced to avoid a hardware revolution…

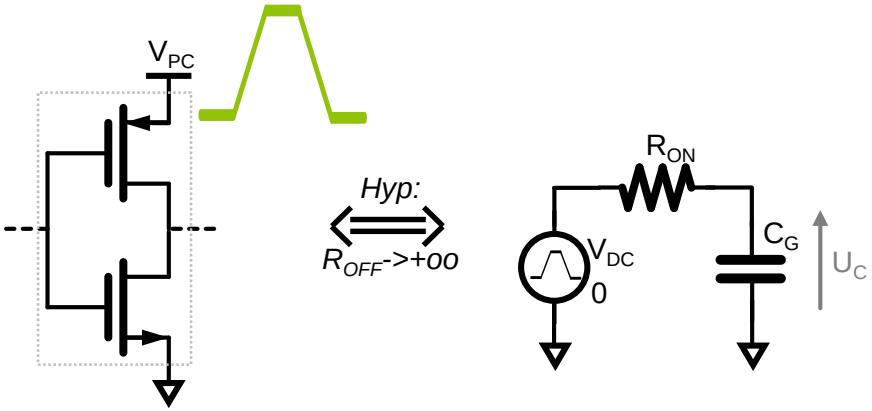


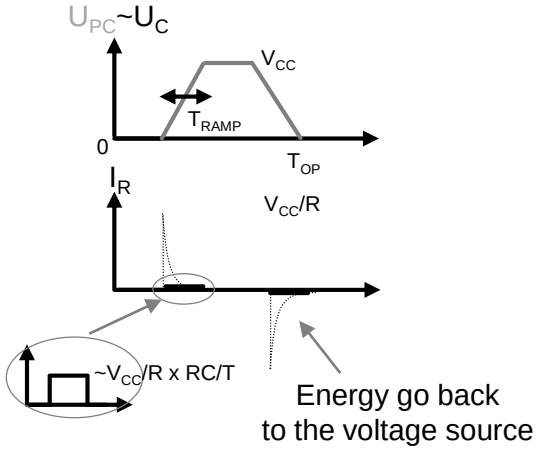
Basic idea:
only replace a DC-power supply V_{DC}
by a trapezoidal power-clock V_{PC}



ADIABATIC ENERGY GAIN AND LIMITATION WITH FET

Go back to the energy transfer basic, but with “soft charging”





$$E_{V_{PC}} = \int_{t=0}^{T_{OP}} U_{PC} \times I_{PC} \approx \frac{R_{ON} C_G}{T_{RAMP}} C_G (V_{CC}^2 - V_{TH}^2) + C_G V_{TH}^2 \xrightarrow{T_{RAMP} \gg R_{ON} C_G} C_G V_{TH}^2$$

Controlled inherent *dynamic loss* in adiabatic

Uncontrolled inherent *dynamic loss* due to the FET behavior

ADIABATIC ENERGY ROOT LIMITATION #1

It it really a serious problem?

Quantify this uncontrolled loss in the last node CMOS technology:
$\{V_{CC};C_G\}=\{1V;0.1fF\}$
$\{R_{ON};T_{RAMP}\}=\{1k\Omega,10ps\}$
$V_{TH}=0.3V$ ➔ $E_{OP}=0.01fJ >> 3zJ$

Yes! we are 10^4 higher than the Landauer limit

Why not reduced V_{TH}?

Because we are face to a hardware limitation…

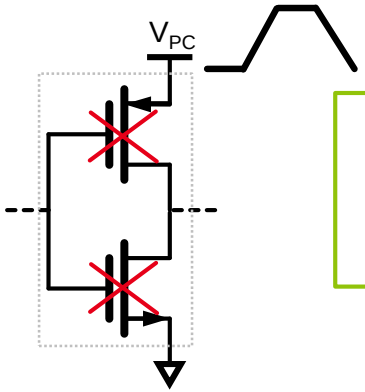
$$E_{V_{PC}} \approx \underbrace{\frac{R_{ON}C_G}{T_{RAMP}} C_G(V_{CC}^2 - V_{TH}^2) + C_G V_{TH}^2}_{\textit{dynamic}\ \text{loss}\ \ f(V_{TH})} + \underbrace{I_{OFF}V_{CC}T_{RAMP}}_{\textit{static}\ \text{loss}\ \ f\left(\frac{1}{V_{TH}}\right)}$$

An inherent trade-off for any semiconductor device between its cut-off and on-state strength exits

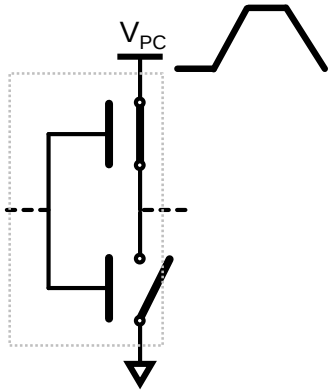
WHAT'S NEXT?

Adiabatic technique is efficient but not using FET devices.
We need a hardware revolution!

Fortunately, the *mechanical device* has been (re)introduced*…

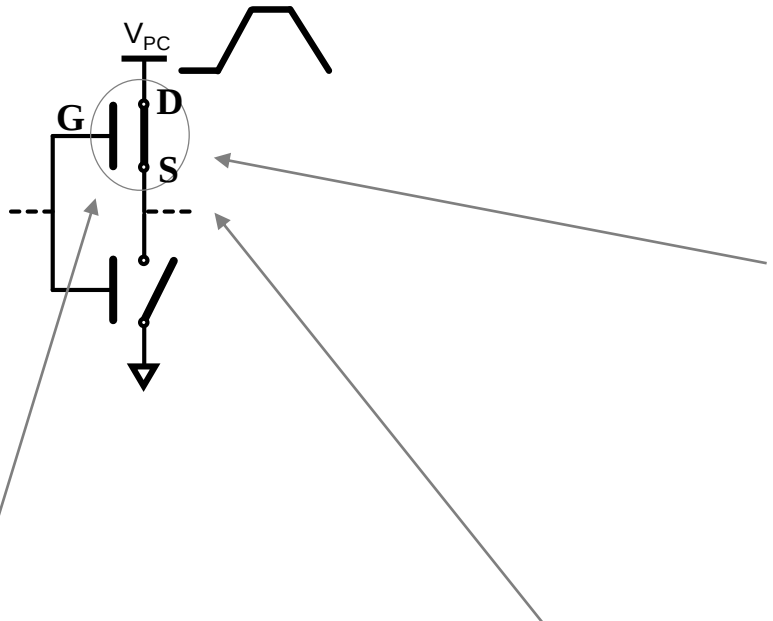


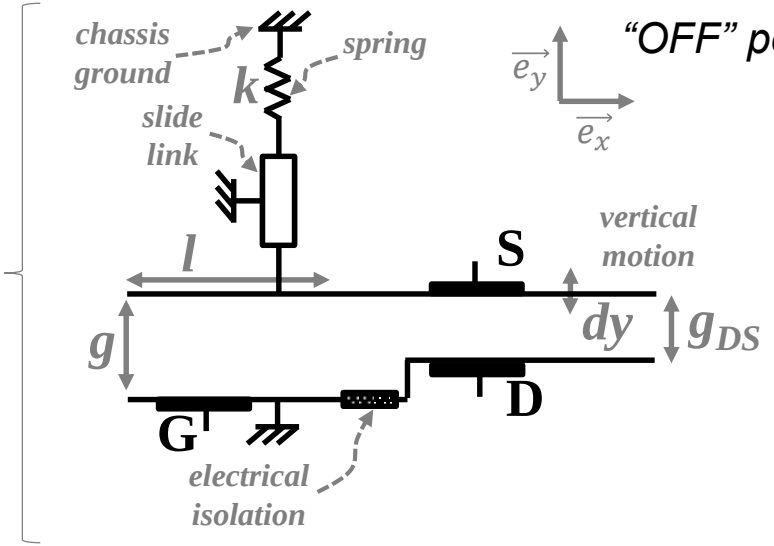
Basic idea:
Use metal contact (or no contact)
to have not I_{ON} over I_{OFF} compromise



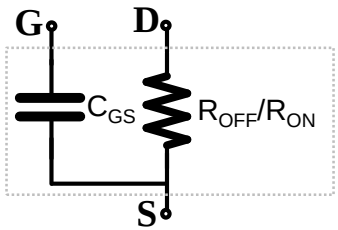
** in combination with adiabatic technique*

HOW TO FABRICATE RELAYS?

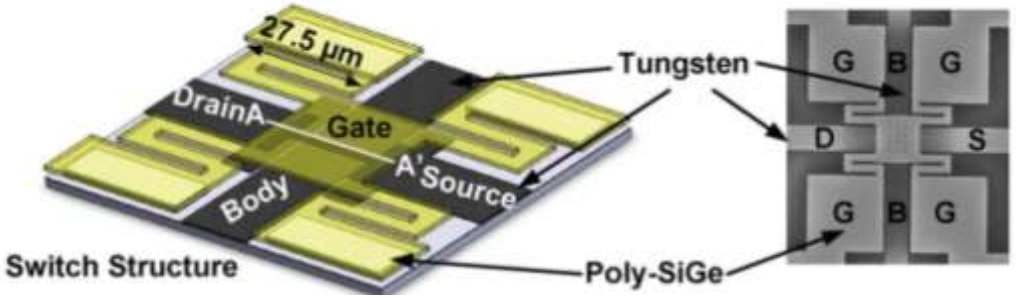




Simplified mechanical scheme



Equivalent electrical model



µ-relay fabricated

** M. Spencer, "Demonstration of Integrated Micro-ElectroMechanical Relay Circuits for VLSI Applications", JSSCC, 2011*

ENERGY DISSIPATION USING MEMS RELAYS

$$E_{V_{PC}} = \int_{t=0}^{T_{OP}} U_{PC} \mathrm{x} I_{PC} \approx \frac{R_{ON} C_G}{T_{RAMP}} C_G (V_{CC}^2 - V_{PO}^2) + C_G V_{PO}^2 \xrightarrow[T_{RAMP} \gg R_{ON} C_G]{} C_G V_{PO}^2$$

Controlled inherent *dynamic loss* in adiabatic

Still uncontrolled inherent *dynamic loss* in adiabatic based on relay

Quantify for nano-scale relay:
$\{U_{PI};U_{PO}\}=\{10mV;1mV\}$
$\{V_{CC};C_G\}=\{1V;100pF\}$
$\{R_{ON};T_{RAMP}\}=\{10k\Omega,100\mu s\}$ ➔ $E_{OP}=0.1fJ$

No, we are still 10^4 higher than the Landauer limit
with $x10^{10}$ operating period and $x10^6$ size compared to MOS

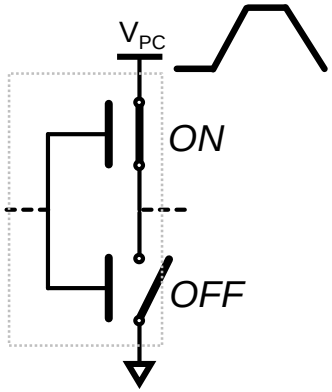
+ technological limitation:
mechanical reliability due to the bad electrical contact and chocks…

WHAT'S NEXT?

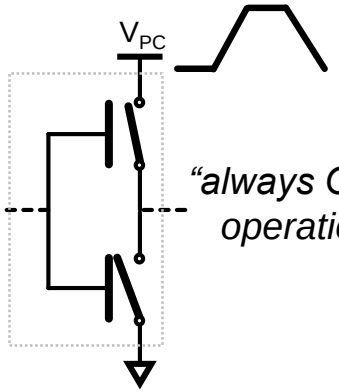
Go back to our old MOS transistors
or try another revolution to save energy?

OR

Fortunately, the *capacitive adiabatic logic* is introduced! [1]



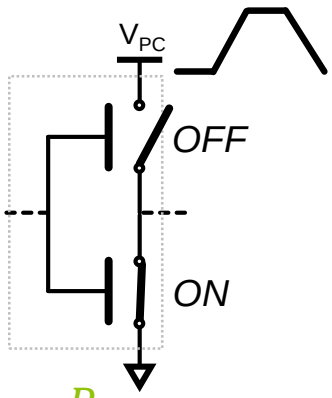
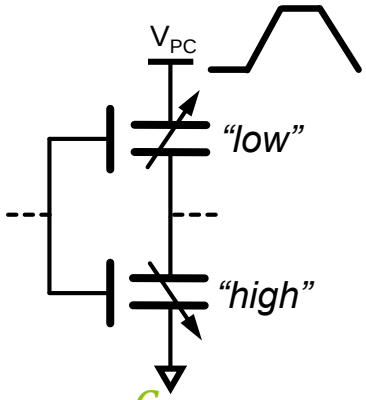
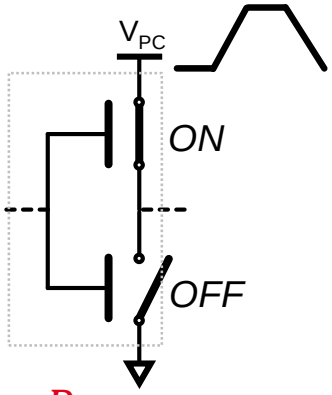
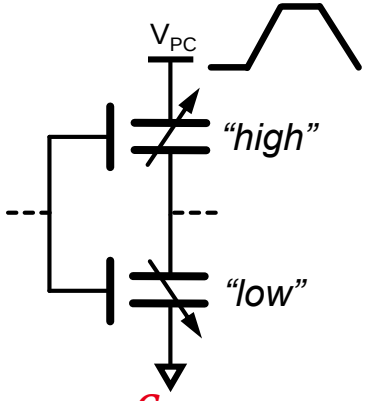
Basic idea:
use relay
but in (electrical) contactless operation
and adiabatic operation



[1] G. Pillonnet, S. Houri and H. Fanet, "Adiabatic Capacitive Logic: a paradigm for low-power logic," IEEE ISCAS, 2017

HOW TO USE CONTACTLESS RELAYS?

Relays become variable capacitors in CAL paradigm

Buffer example		
"0" logic input	 $V_o = \frac{R_{ON}}{R_{OFF} + R_{ON}} V_{PC} \sim 0$	 $V_o = \frac{C_L}{C_H + C_L} V_{PC} \sim 0$
"1" logic input	 $V_o = \frac{R_{OFF}}{R_{OFF} + R_{ON}} V_{PC} \sim V_{PC}$	 $V_o = \frac{C_H}{C_L + C_H} V_{PC} \sim V_{PC}$

Trade resistive divider for capacitive one

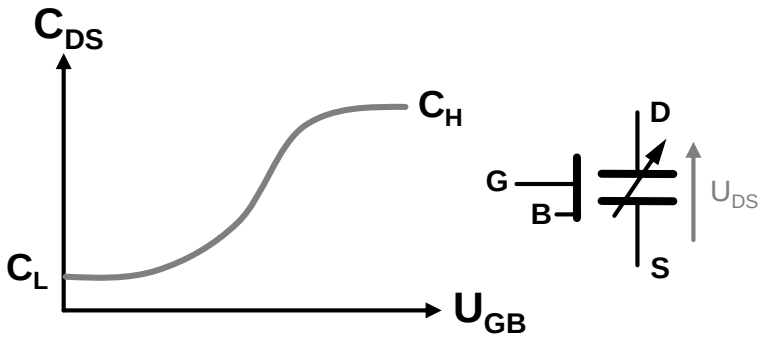
WHO IS THE ELEMENTARY DEVICES IN CAL?

Positive- and negative- variable capacitors (VC)
are the elementary hardware device in CAL

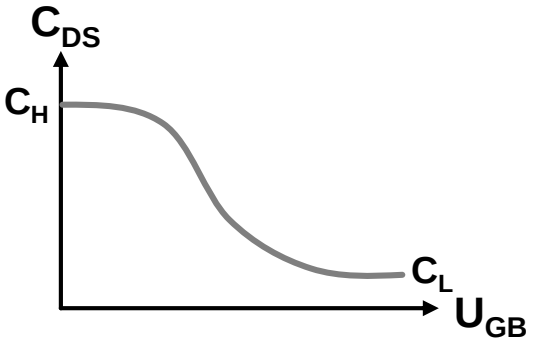
MOS	relay	VC
P-MOS		P-CV
N-MOS		N-CV

Analogy to transistor-, relay-based logic

P-CV
C(V) curve



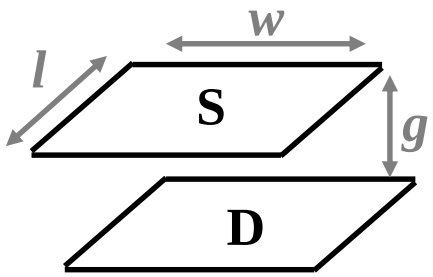
N-CV
C(V) curve



HOW TO IMPLEMENT VC DEVICES

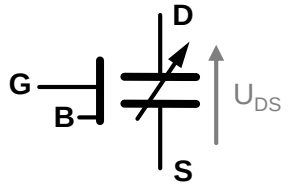
How to change a capacitor value?

$$C_{DS} = \varepsilon_0 \varepsilon_r \frac{w \times l}{g}$$



By changing surface ($w_x l$), gap between plates (g) or permittivity (ε_r)

C_{DS} changes by an isolated voltage U_{GB}
➔ it is a <u>four</u> terminals device

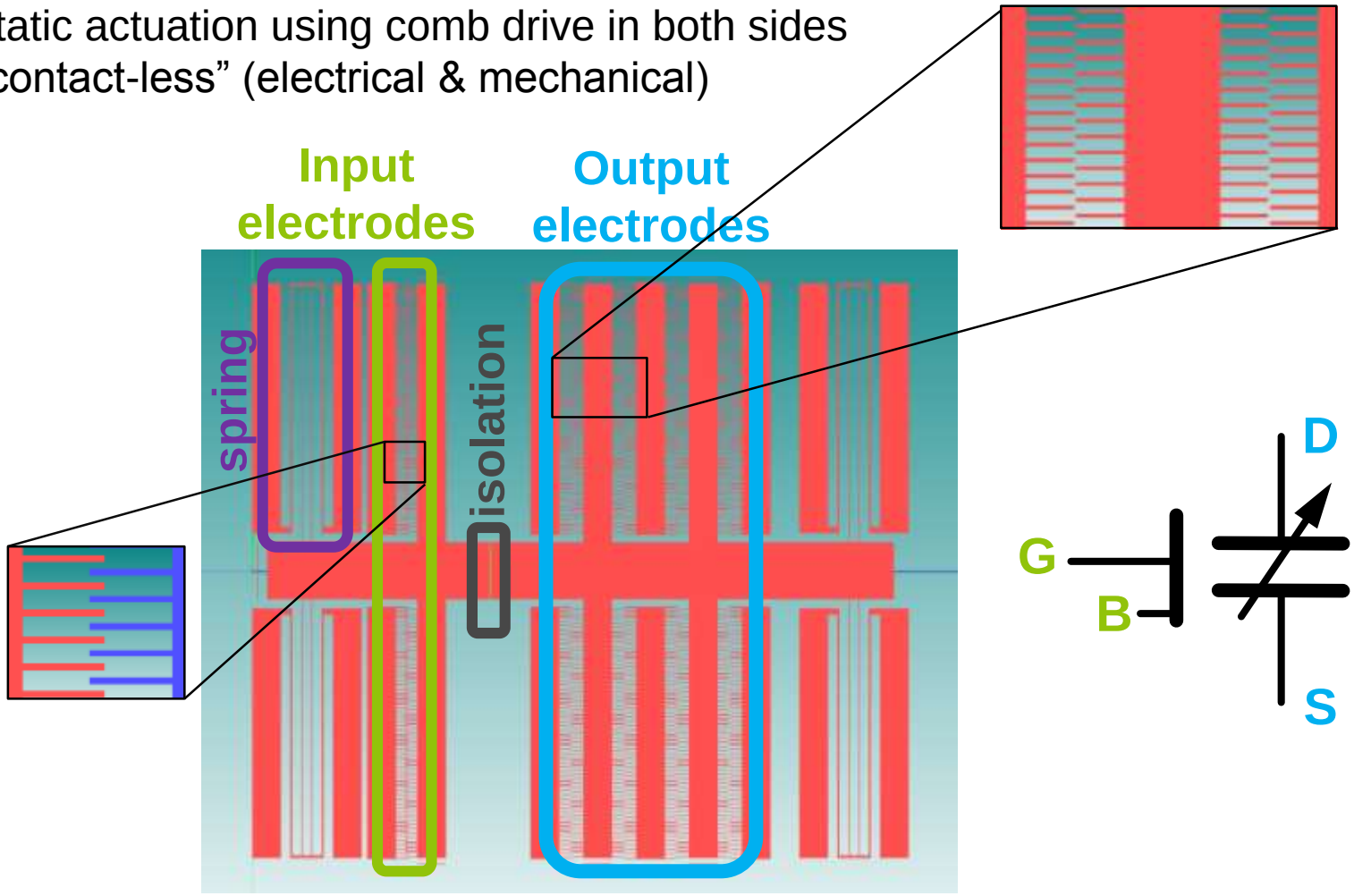


Actuation could be :

- Thermal ➔ not very reversible…
- Piezoelectric ➔ trade off between leakage and dynamic losses
- Electrodynamic ➔ current actuation
- Electrostatic ➔ small gap needed to have reasonable supply voltage

PROPOSED HARDWARE SOLUTION*

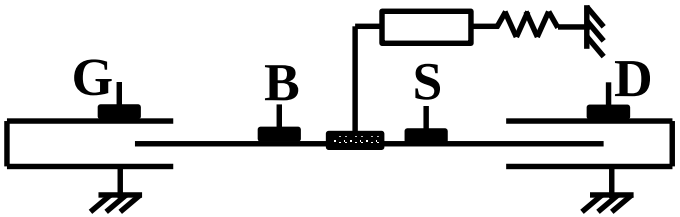
Well known MEMS topology (~excepted isolation)
Electrostatic actuation using comb drive in both sides
Purely “contact-less” (electrical & mechanical)



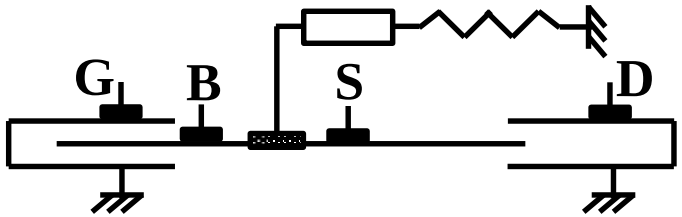
** This is not the only hardware solution to implement a 4-terminal variable cap’*

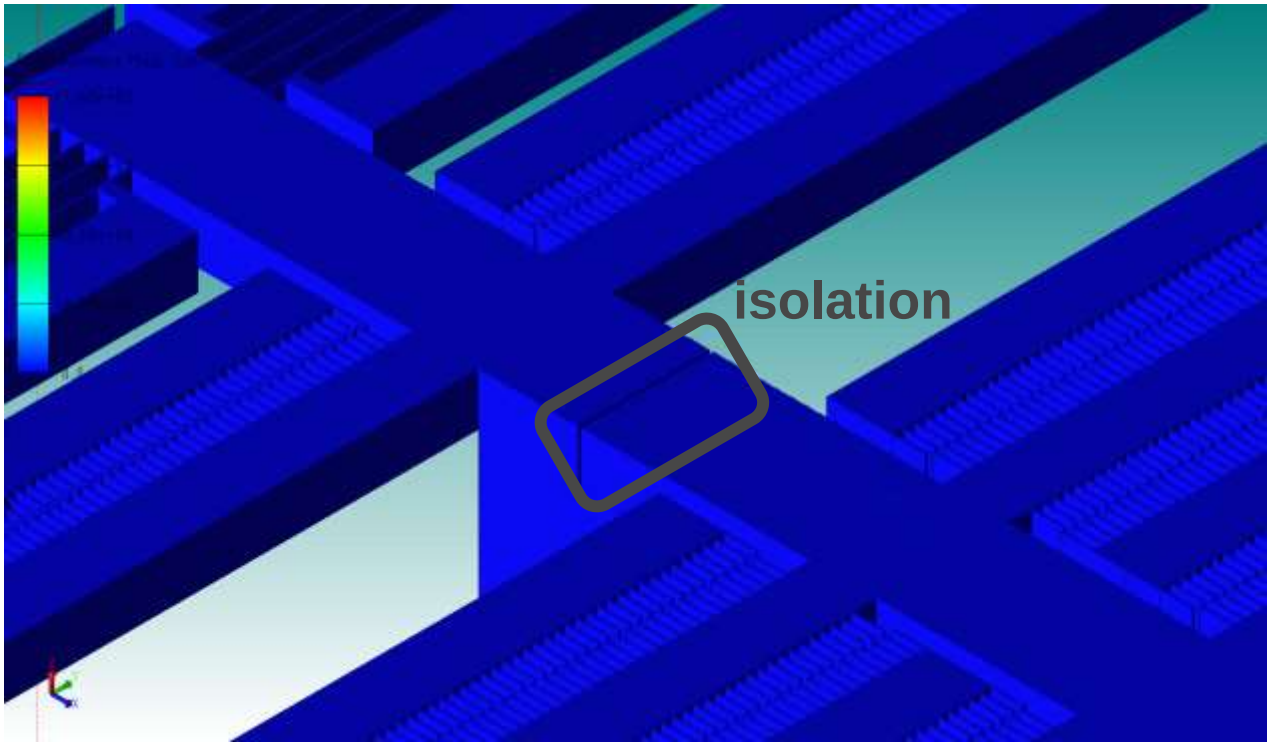
DISPLACEMENT AGAINST INPUT VOLTAGE

“low” position



“high” position (V_{GB}>0)



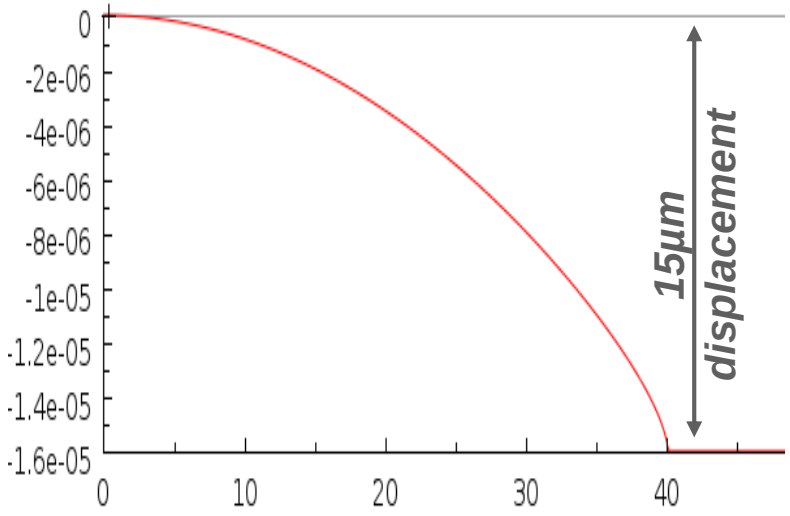


Simulation from Coventor, MEMS+

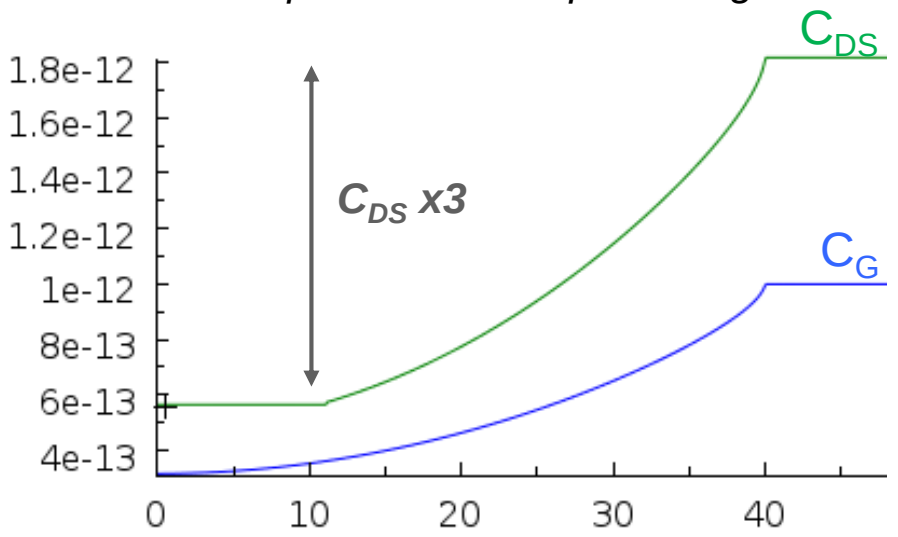
ELECTROMECHANICAL CHARACTERISTICS

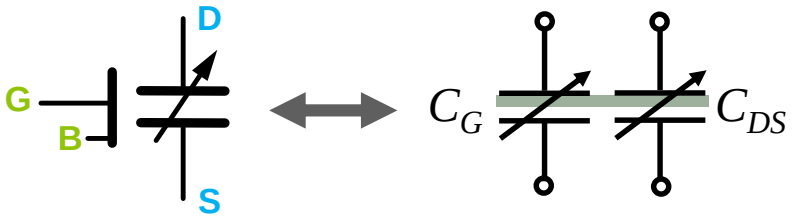
The MEMS sizing is given by cascability logic constraints (see later)

Displacement against input voltage



Capacitance vs input voltage





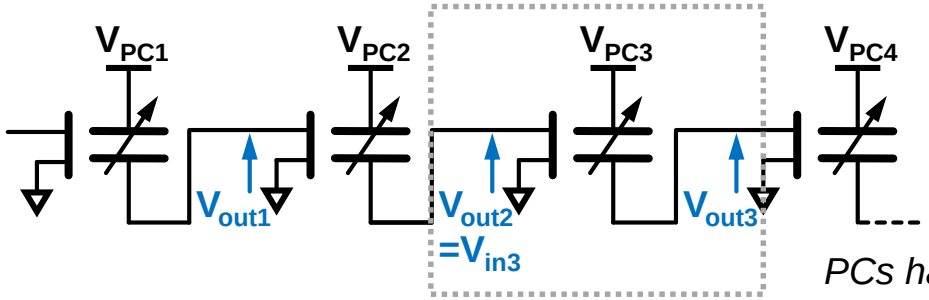
2 caps mechanically coupled

$$i(t) = \underbrace{C(x)\frac{dV(t)}{dt}}_{\text{electrical part}} + \underbrace{\frac{dC(x)}{dx}V\frac{dx}{dt}}_{\text{mechanical part}}$$

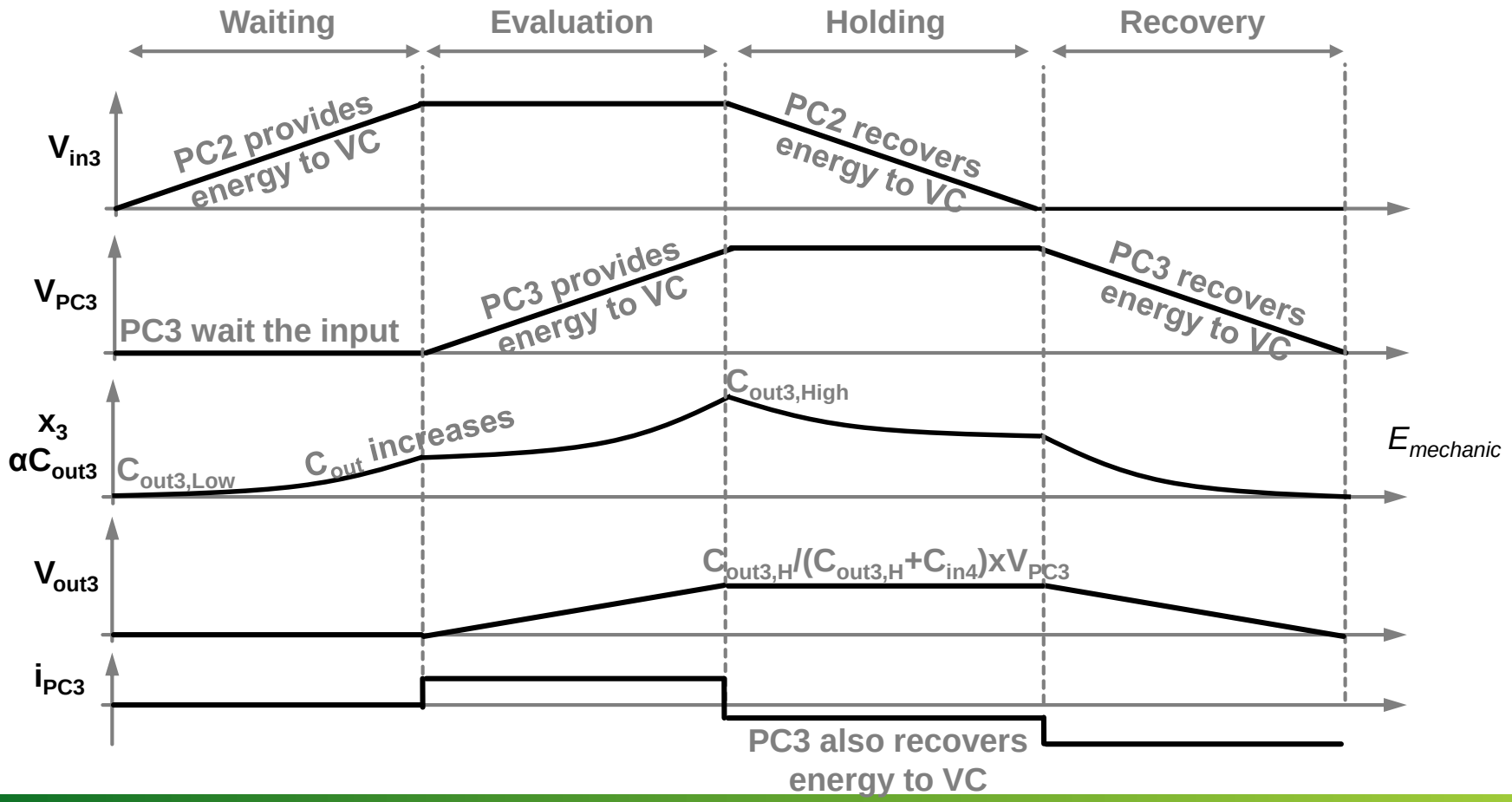
Simulation from Coventor, MEMS+ for 1mm² device (2µm gap)

BUFFER BEHAVIOR: STEP BY STEP

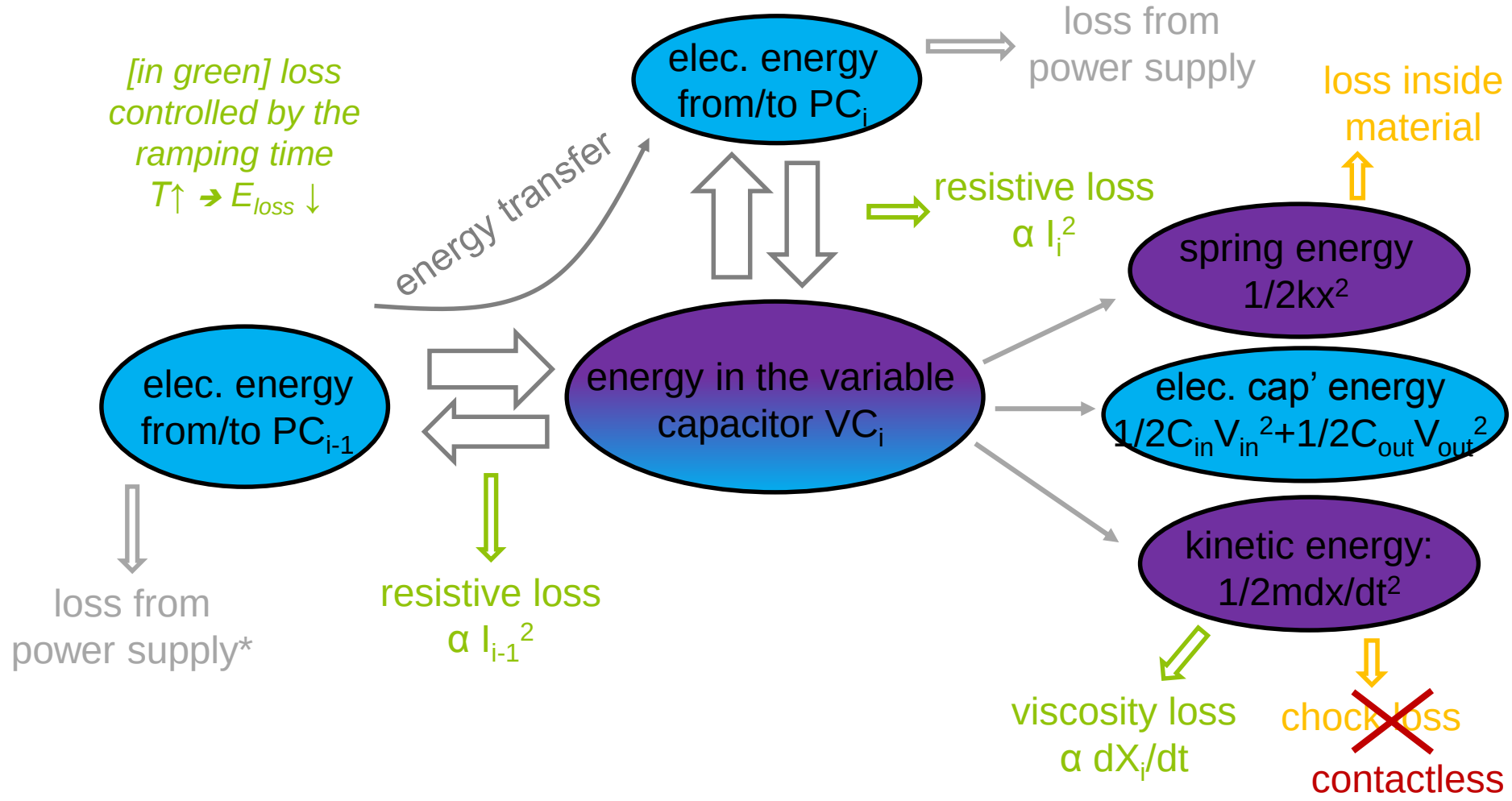
Buffer pipeline



PCs have a π/2 phase shift

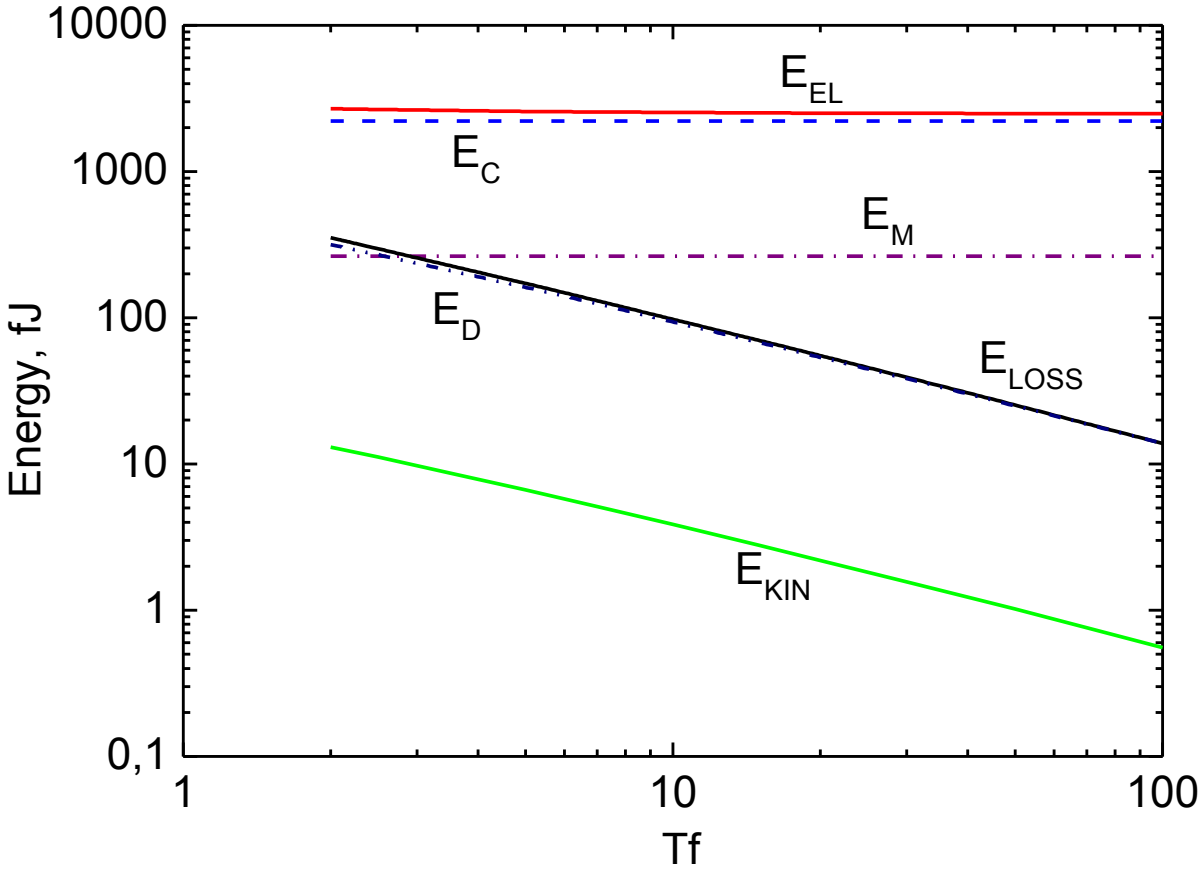


BUFFER BEHAVIOR: ENERGY TRANSFER



** Power supply must be reversible and AC (literature has already proved high efficiency power supplies)*

(OUR) "ADIABATIC LOSS" DEFINITION



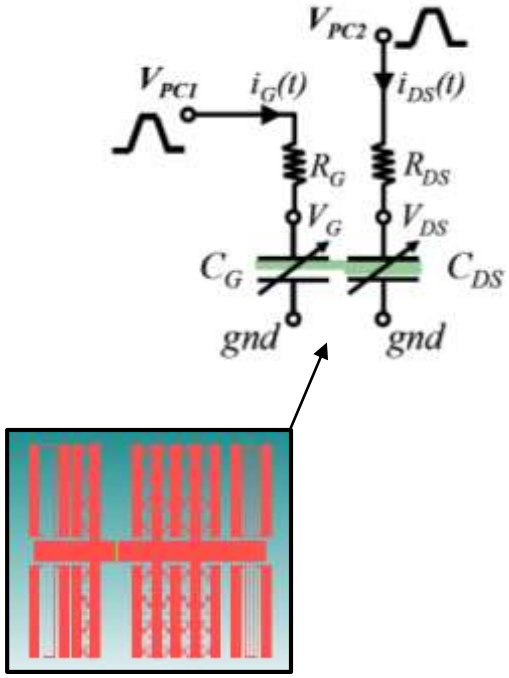
Definition:
loss scaling linearly with the ramping time

Need low dissipation?
Reduce the speed!

Here, our MEMS moving is always controlled by the power clock ramping time

"Gap closing" MEMS is not suitable as motion is not controlled after the pull-in

ENERGY ANALYSIS OF ELEMENTARY MOVING

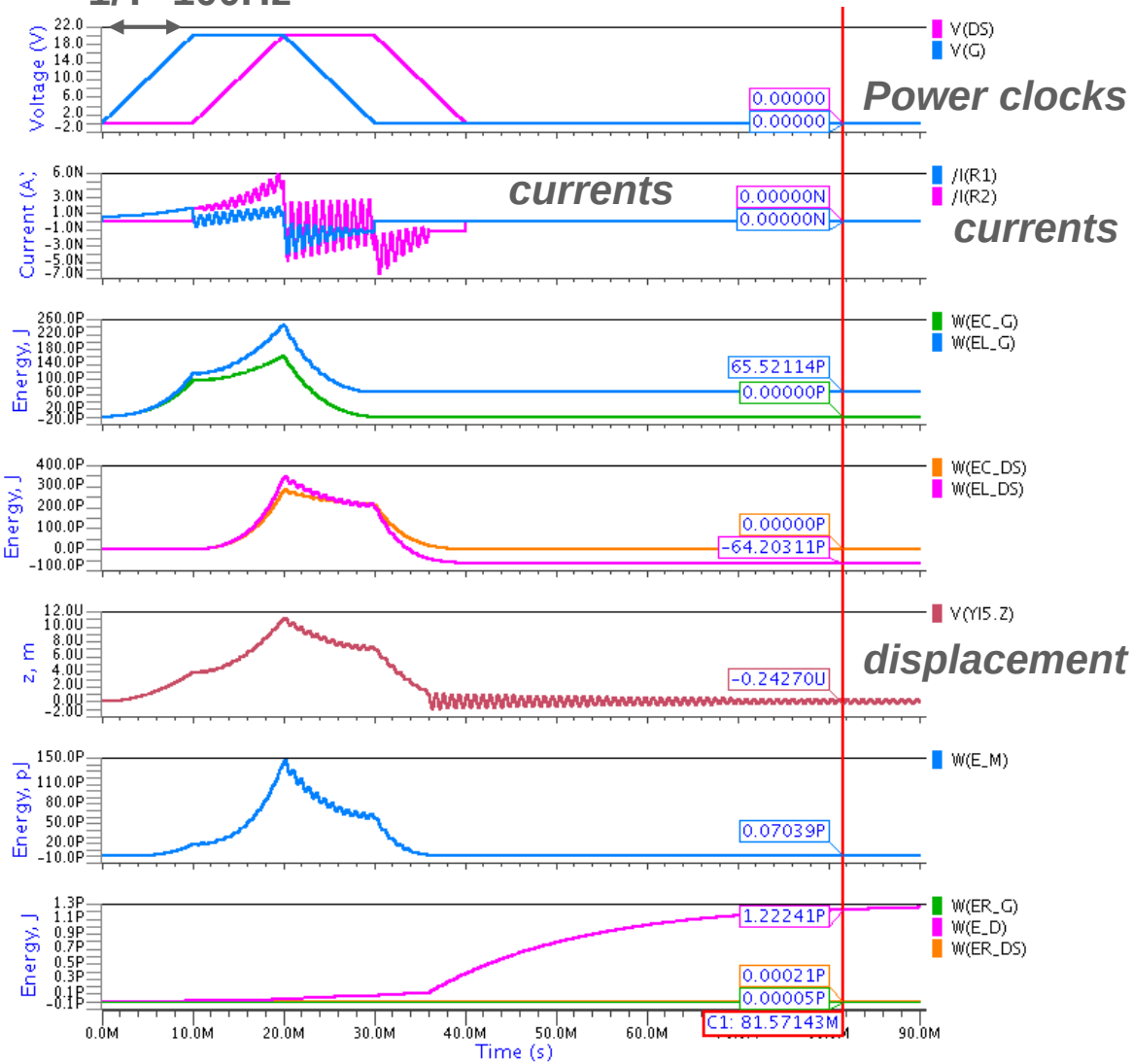


$E_{OP,min}$=1,2pJ pour 1mm²

(vs 1fJ for nano-scale transistor)

thanks to the controlled moving and energy back

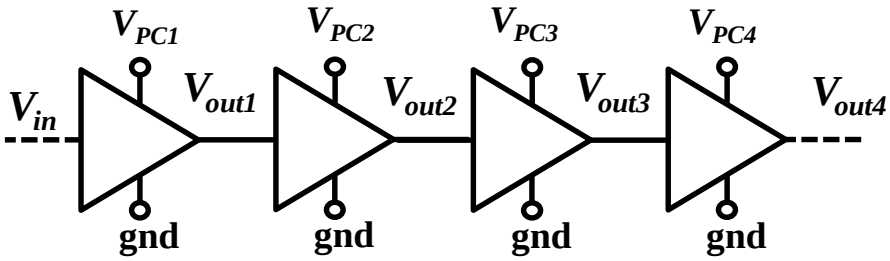
1/T=100Hz

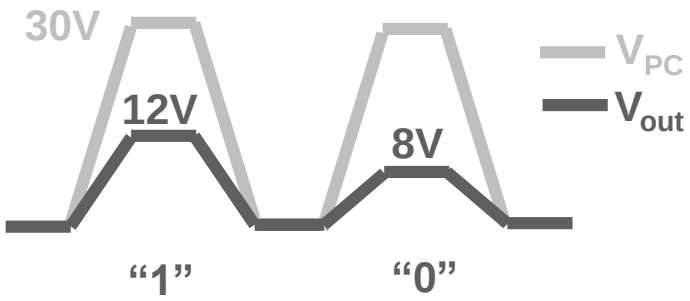


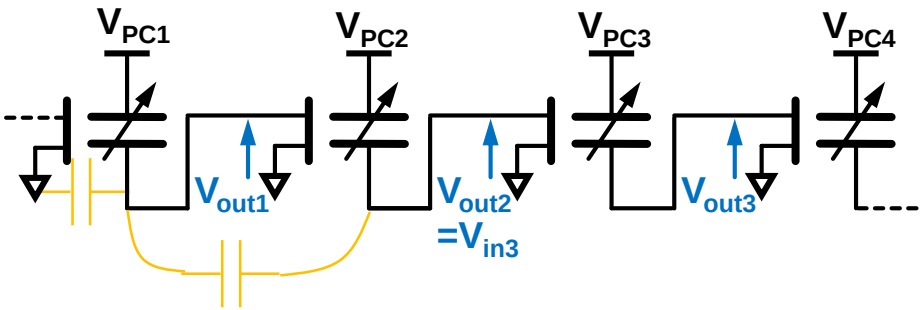
Electrical simulation using simplified model (VHDL-AMS)

LOGIC PROPAGATION THROUGH PIPELINE

The biggest issue: find the right MEMS configuration (cap variation, C_{in} vs C_{out}…) to propagate the logic state gate by gate

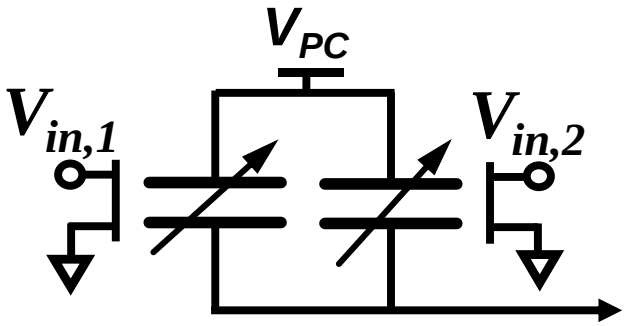




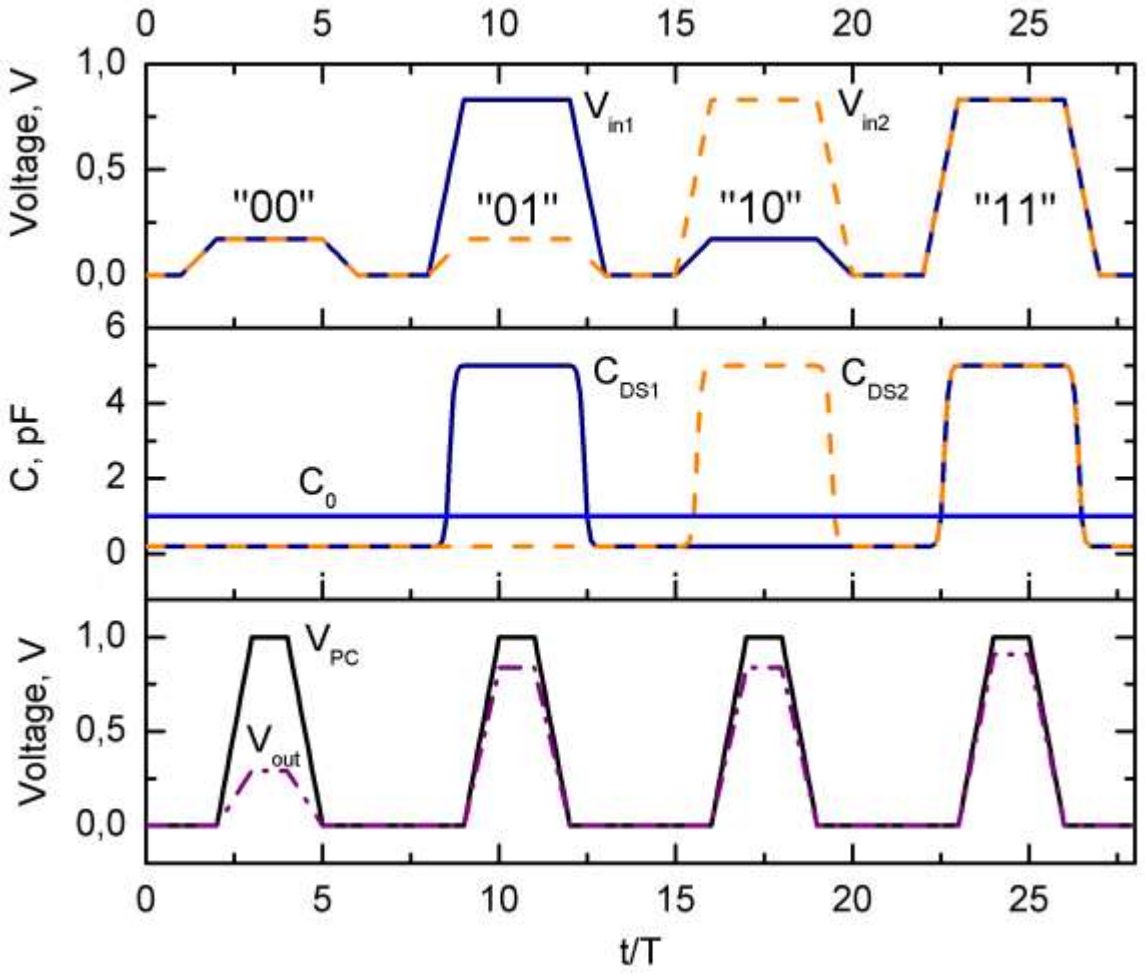


Cascability condition
= have different voltage levels
Occurred when 30V < V_{PC} < 37V

LOGIC OPERATION: OR EXAMPLE



to the next gate

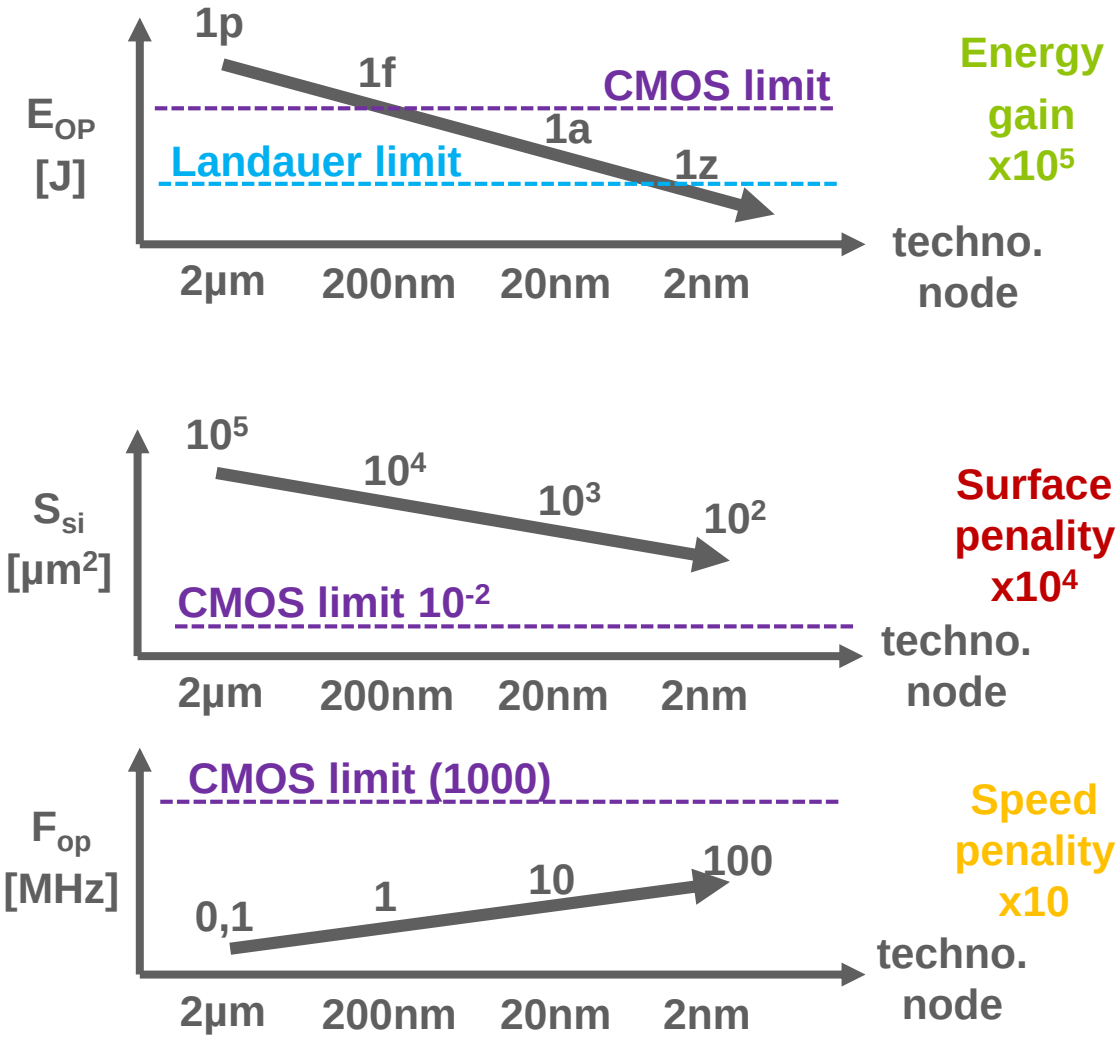


All combination logic operation is possible with CVP and/or CVN devices

ROADMAP FOR DEEPER INTEGRATION

Based on the current (first draft) MEMS…

Gap	1/k
Linear sizes	1/k
Mass	$1/k^3$
Spring constant	k
Frequency	k
Capacitance	1/k
Actuation voltage	1/k
E_{LOSS}	$1/k^3$



Targeted application: low processing rate with high energy constraint (e.g. autonomous environmental sensors)

THANKS TO THE TEAM

Hervé Fanet

Gaël Pillonnet

Louis Hutin

Bruno Reig

Full time researchers in Léti (Grenoble, France)

Gregory Snider
Prof. Univ. of Notre Dame

Samer Houri
Delft Tech.Univ.

External partners

Ayrat Galisultanov
post doc.

Yann Perrin
post doc.

Post PhD

CONCLUSION

Actual CMOS logic is an “energy heresy” for logic operation
The root of the problem is the elementary gate behavior
➔ New device / design style at the gate level has to be invented!

Adiabatic design style is promising but we need a dedicated device, not FET
➔ variable capacitor (VR) seems to be “adiabatic compatible”

This is preliminary results waiting the silicon device measurements…

Contact-less variable capacitors could be based on:
- well-known MEMS structures with already proved scalability and reliability abilities
- Other (reversible) actuation: to be defined!

Beware: every solution has to be cascadable *(propagate logic state to the next stage)*

It is not a crazy alternative to reduce the energy dissipation…

Open question: where is the energy limit using the proposed MEMS?

Your feedbacks are more than welcome!

CAPACITIVE ADIABATIC LOGIC: A NEW PARADIGM FOR LOW-POWER COMMUTATION

Microenergy, Gubbio, Italy
Gaël Pillonnet | July 2017